

LISTING OF CLAIMS

The listing of claims below replaces all prior versions, and listings, of claims:

- 1 1. (Previously Presented) A system comprising:
 - 2 a memory bus; and
 - 3 a plurality of memory controllers, each memory controller to generate
 - 4 memory requests on the memory bus according to a predetermined priority scheme, the
 - 5 predetermined priority scheme defining time slots, wherein the memory controllers are
 - 6 allocated to respective time slots according to the predetermined priority scheme,
 - 7 at least two of the plurality of memory controllers adapted to generate
 - 8 concurrently pending memory requests on the memory bus in plural respective time slots.

- 1 2. - 4. (Cancelled)

- 1 5. (Original) The system of claim 1, wherein each memory controller
2 generates a memory request during a different predetermined time slot.

- 1 6. (Original) The system of claim 1, wherein the memory bus comprises
2 plural control portions, each of the control portions associated with corresponding time
3 slot priority schemes.

- 1 7. (Original) The system of claim 6, wherein the time slot priority schemes
2 are staggered.

- 1 8. (Original) The system of claim 6, wherein the control portion comprise a
2 row portion and a column portion.

- 1 9. (Original) The system of claim 1, wherein the memory bus comprises
2 plural portions, each portion associated with a set of memory devices.

1 10. (Previously Presented) A system comprising:
2 a plurality of memory buses;
3 a hub connected to the plurality of memory buses; and
4 a plurality of memory controllers connected to a first one of the memory
5 buses, each memory controller to monitor memory requests generated by another
6 memory controller in performing memory-related actions,
7 the memory controllers to access a second one of the memory buses
8 through the hub.

1 11. (Original) The system of claim 10, wherein the memory-related actions
2 comprise a read-modify-write transaction.

1 12. (Original) The system of claim 10, wherein the memory-related actions
2 comprise a cache coherency action.

1 13. (Original) The system of claim 10, wherein the memory-related actions
2 comprise a memory request.

1 14. (Previously Presented) The system of claim 10, each memory controller to
2 determine if the memory buses are available based on outstanding requests from other
3 memory controllers.

1 15. (Previously Presented) A method for use in a system having plural
2 memory buses, a hub connected to the memory buses, and a plurality of memory
3 controllers, the method comprising:
4 generating requests, by the memory controllers, on the memory buses; and
5 each memory controller monitoring memory-related actions on the
6 memory buses connected by the hub by at least another memory controller.

1 16. (Original) The method of claim 15, wherein generating the requests
2 comprises generating Rambus command packets.

1 17. (Original) The method of claim 15, wherein generating the requests
2 comprises the memory controllers generating the requests one at a time according to a
3 predetermined priority scheme.

1 18. (Original) The method of claim 17, wherein generating the requests
2 comprises generating the requests according to a time slot priority scheme.

1 19. (Original) The method of claim 17, wherein generating the requests
2 comprises generating the requests according to a request-select priority scheme.

1 20. (Previously Presented) The method of claim 15, further comprising each
2 memory controller determining when to generate a memory request based on the
3 monitoring.

1 21. (Previously Presented) The method of claim 15, further comprising each
2 memory controller determining if a lock has been asserted due to presence of a read-
3 modify-write transaction.

1 22. (Previously Presented) The method of claim 15, further comprising each
2 memory controller performing a cache coherency action based on the monitoring.

1 23. (Previously Presented) An article comprising one or more storage media
2 containing instructions that when executed cause a memory controller to:
3 monitor memory requests from another memory controller on a memory
4 bus;
5 determine if a memory request can be generated on the memory bus based
6 on the monitoring; and
7 generate memory requests on the memory bus according to a time slot
8 priority scheme that defines time slots allocated to respective memory controllers.

1 24. (Previously Presented) The system of claim 1, wherein the plurality of
2 memory controllers are connected to the memory bus.

1 25. (Previously Presented) The system of claim 1, wherein one of the at least
2 two memory controllers is adapted to generate its memory request on the memory bus
3 before data is returned for the memory request of the other one of the at least two
4 memory controllers.

1 26. (Previously Presented) The system of claim 10, wherein at least two of the
2 memory controllers are adapted to generate concurrently pending memory requests on the
3 first memory bus, each of the concurrently pending memory requests comprising control
4 information and memory address information.

1 27. (Previously Presented) The system of claim 26, wherein one of the at least
2 two memory controllers is adapted to generate its memory request including control
3 information and memory address information on the memory bus before data is returned
4 for the memory request of the other one of the at least two memory controllers.

1 28. (Previously Presented) The method of claim 15, wherein generating the
2 requests on the memory bus comprises at least two of the memory controllers generating
3 concurrently pending requests on the memory bus, each of the concurrently pending
4 requests comprising control information and memory address information.

1 29. (Previously Presented) The method of claim 28, wherein generating
2 concurrently pending requests comprises one of the at least two memory controllers
3 generating its request including control information and memory address information on
4 the memory bus before data is returned for the request of the other of the at least two
5 memory controllers.

1 30. (Previously Presented) The article of claim 23, wherein the memory
2 controllers are connected to the memory bus.

1 31. (Previously Presented) The system of claim 1, wherein the predetermined
2 priority scheme enables the memory controllers to gain access to the memory bus without
3 having to assert arbitration requests.

1 32. (Previously Presented) The system of claim 1, wherein the memory
2 controllers are adapted to access the memory bus according to a round-robin priority
3 scheme.

1 33. (Previously Presented) The system of claim 1, wherein the memory bus
2 comprises a first memory bus, the system further comprising:

3 a hub connected to the first memory bus; and
4 a second memory bus connected to the hub, at least two of the memory
5 controllers adapted to generate concurrently pending memory requests on the second
6 memory bus through the hub.

1 34. (Previously Presented) The system of claim 33, wherein each of the
2 memory requests comprises control information and memory address information, the at
3 least two memory controllers adapted to generate concurrently pending memory requests
4 on the second memory bus by providing control information and memory address
5 information of the concurrently pending memory requests on the second memory bus.

1 35. (Previously Presented) The system of claim 33, wherein each of the
2 memory requests comprises control information and memory address information, the at
3 least two memory controllers adapted to generate concurrently pending memory requests
4 on the first memory bus by providing control information and memory address
5 information of the concurrently pending memory requests on the first memory bus.

1 36. (Previously Presented) The system of claim 10, wherein the plurality of
2 memory controllers are each adapted to generate memory requests on the first one of the
3 memory buses, each memory controller to monitor memory requests on the first one of

4 the memory buses generated by another memory controller on the first one of the
5 memory buses.

1 37. (Previously Presented) The system of claim 10, wherein the plurality of
2 memory controllers are each adapted to generate memory requests on the second one of
3 the memory buses, each memory controller to monitor memory requests on the second
4 one of the memory buses generated by another memory controller on the second one of
5 the memory buses.

1 38. (Previously Presented) The system of claim 37, wherein the memory
2 controllers are adapted to access any of the memory buses according to a time slot
3 priority scheme that defines a plurality of time slots allocated to respective memory
4 controllers.

1 39. (Previously Presented) The system of claim 38, wherein the memory
2 controllers are adapted to access any of the memory buses according to the time slot
3 priority scheme without asserting arbitration requests.

1 40. (Previously Presented) The system of claim 10, further comprising
2 memory devices connected to respective memory buses, the memory devices accessible
3 by the memory controllers.

1 41. (Previously Presented) The system of claim 11, wherein a first one of the
2 memory controllers is adapted to generate the read-modify-write transaction, the first one
3 of the memory controllers to assert a lock indication for a memory location accessed by
4 the read-modify-write transaction to prevent another one of the memory controllers from
5 accessing the memory location.

1 42. (Previously Presented) The method of claim 15, further comprising:
2 the plurality of memory controllers generating memory requests on a first
3 one of the memory buses; and

4 each memory controller monitoring memory requests on the first one of
5 the memory buses generated by another memory controller on the first one of the
6 memory buses.

1 43. (Previously Presented) The method of claim 15, further comprising:
2 the plurality of memory controllers generating memory requests on a
3 second one of the memory buses through the hub; and
4 each memory controller monitoring memory requests on the second one of
5 the memory buses generated by another memory controller on the second one of the
6 memory buses.

1 44. (Previously Presented) The article of claim 23, wherein generating
2 memory requests on the memory bus according to the time slot priority scheme is
3 performed without generating arbitration requests.